

METANOIA

HW TEAM TEST DOCUMENT

2013

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Chapter 1

MT2301

1.1 Power for MT2301

1.1.1 Power Consumption

Profile: 17a
SNR: 6dB
Side: CPE
Mode: Interleave

V Chip	3.3V		1.2V	
	Min	Max	Min	Max
MT2301	20	30	276	308

Table 1.1: MT2301 Power Consumption for 17a Profile Unit in mA.

Profile: 30a
SNR: 6dB
Side: CPE
Mode: Interleave

V Chip	3.3V		1.2V	
	Min	Max	Min	Max
MT2301	40	40	338	376

Table 1.2: MT2301 Power Consumption for 30a Profile Unit in mA.

1.1.2 Power on Sequence

MT2301:No power on sequence requirement.

1.1.3 Power Noise

The power noise of each voltage should be below 75 mV.

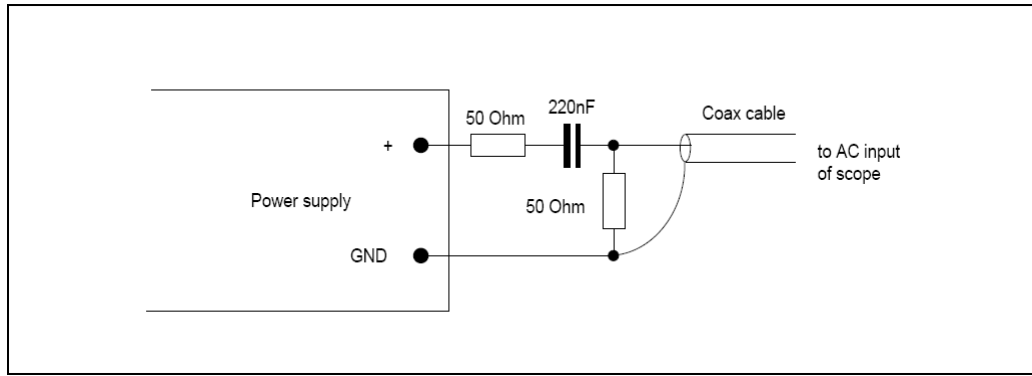


Figure 1.1: Preferred Method to Test Output Noise and Ripple.

1.2 System Clocks

Merlin chipset needs two system clocks for system operation, 25MHz clock is used for DMT and 35.328MHz is clock used for AFE.

1.2.1 System Clocks for MT2301

The MT2301 need a 25MHz oscillator or external crystal resonator and two tuning capacitor as in reference schematic shown in Figure 1.2. The two tuning capacitors, C1 and C2 are corresponding to crystal loading capacitance, for example crystal specification loading capacitance use $18\text{pF} \pm 0.2\text{pF}$ /NPO dielectric. It is recommended to make sure the 25MHz jitter is smaller than 100 ps.

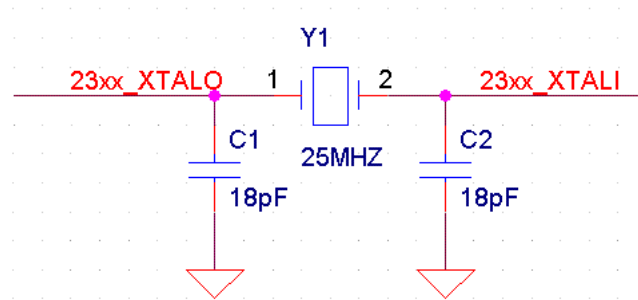


Figure 1.2: Reference Schematic for MT2301 Crystal.

1.3 Interfaces for MT2301

This section describes the MT2301 interfaces, including management interfaces (SPI/HPI) and data interfaces (MII).

1.3.1 SPI

The Serial Peripheral Interface (SPI) is a synchronous serial data, that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

SPI flash		MT2301
CS_n	←	SC2B(pin 84)
SCK	←	SCKB(pin 81)
SI	←	STDB(pin 82)
SO	→	SRDB(pin 83)

Table 1.3: SPI Master Boot.

1.3.2 HPI

HPI bus (Host Port Interface bus) is a flexible interface that enables a micro processor to use the interface to load firmware and manage the MT2301. Through the HPI bus a micro processor can access VDSL MIBs and there through get/set VDSL status.

Micro Processor		MT2301
CPU_CS_n	→	HP_CS(pin 108)
CPU_OE_n	→	HP_RD(pin 109)
CPU_WE_n	→	HP_DS (pin 110)
Data_7	↔	EX_D7/15 (pin 122)
Data_6	↔	EX_D6/14(pin 121)
Data_5	↔	EX_D5/13 (pin 118)
Data_4	↔	EX_D4/12 (pin 117)
Data_3	↔	EX_D3/11 (pin 116)
Data_2	↔	EX_D2/10 (pin 113)
Data_1	↔	EX_D1/9(pin 112)
Data_0	↔	EX_D0/8(pin 111)

Table 1.4: Interface between MT2301 and Processor.

HPI Write Waveform Timing

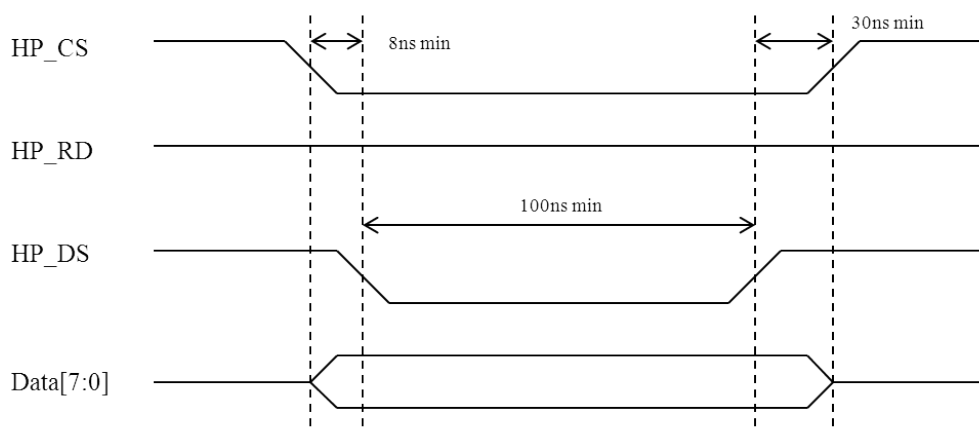


Figure 1.3: HPI Write Timing.

HPI Read Waveform Timing

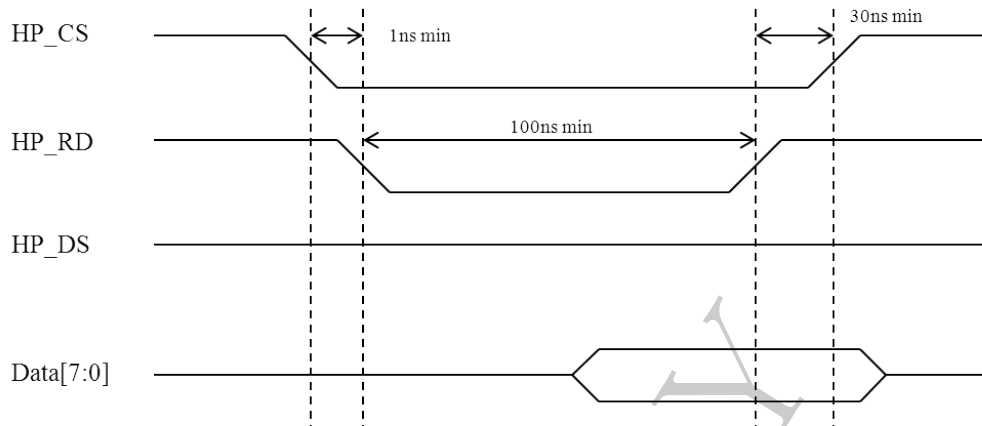


Figure 1.4: HPI Read Timing.

HPI Debugging Step by Step

If implementing control by using HPI and some problems are encountered, the suggested method to debug HPI bus step by step is the following:

1. Set MT2301 boot mode:
 - Set to boot from SPI flash, IRQ[A,B,C,D] to: '0000' or '1111'.
 - MT2301 pin 96 change 10k resistor voltage to 3.3V.
 - Load test firmware to SPI flash use the Eyebox tool to load firmware "HPI_TEST_010201_121109_144714".
2. Access MCU with HPI and do Read/Write testing, each read and write are 8 bytes, timing and sequence are like the following:
 - (a) First of all write the following 8 bytes to the HPI: 00 6c 31 00 00 00 45 71 (no need for extra delay between each byte). Wait 500 μ s, then read 8 bytes back from HPI, if the read action succeeds, the content of the data should be like this: 00 6c 31 01 01 00 41 32 (no need for extra delay between each byte).
 - (b) Those 8 bytes we write into HPI can be verified by using DslMonitor application, open DslMonitor, Monitor variable "HostRxCmdFifo" as in Figure 2.3:

If the writing is successful, the DslMontiot will show the written value. If the value is wrong, please check whether the error is because of HPI timing or because of wrong routes of HPI HW.

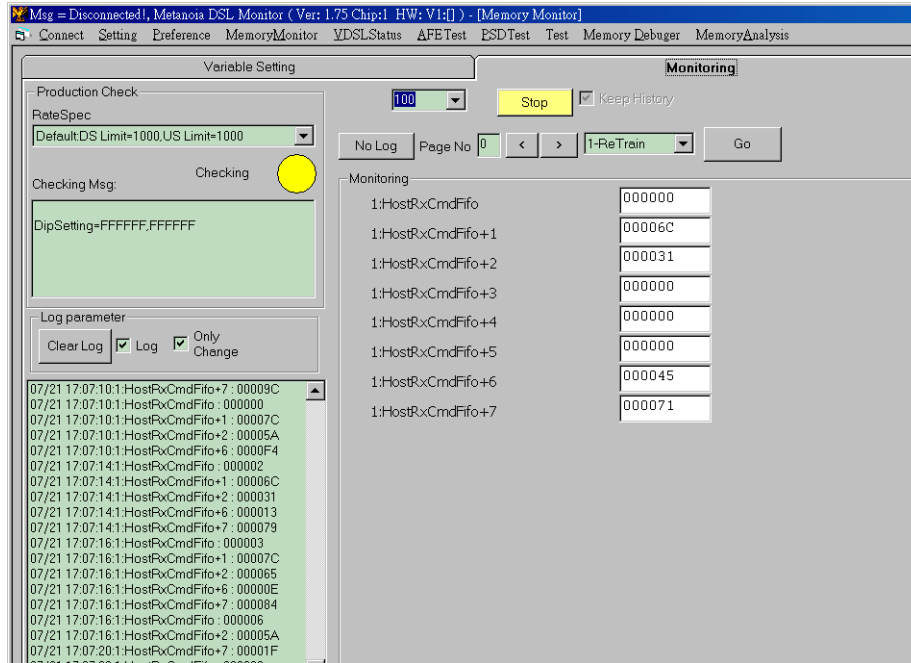


Figure 1.5: HPI Debug Interface.

Boot from HPI Interface

1. Reset MT2301 for 5ms.
2. MT2301 wait 500ms for BIST completed.
3. Load firmware, byte interleave recommended to be $>8\mu s$.
4. Load firmware complete and wait 100ms.
5. Write 8 byte data without inter-byte gap.
6. Wait $300\mu s$.
7. Read 8 byte data with inter-byte gap $>8\mu s$.
8. Wait $300\mu s$.
9. Repeat item 5 to 8 for read/write data.

1.3.3 Ethernet Interfaces

The Media Independent Interface (MII) provides Ethernet connectivity between 10/100 Media Access Control (MAC) and Physical Layer (PHY) devices. MT2301 uses MII in PHY mode and the following figures show how to connect the MII interface with a network processor.

MII (PHY Mode)

Micro Processor / Switch		MT2301
RXDV	←	MII_RXDV(O)
RXCLK	←	MII_RXCLK(O)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
COL	←	MII_COL(O)
CRS	←	MII_CRS(O)
TXEN	→	MII_TXEN(I)
TXCLK	←	MII_TXCLK(O)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)

Table 1.5: MII (PHY Mode) Interface between MT2301 and Processor.

MII (MAC Mode)

Micro Processor / Switch		MT2301
RXDV	←	MII_RXDV(O)
RXCLK	→	MII_RXCLK(I)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
COL	←	MII_COL(O)
CRS	←	MII_CRS(O)
TXEN	→	MII_TXEN(I)
TXCLK	→	MII_TXCLK(I)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)

Table 1.6: MII (MAC Mode) Interface between MT2301 and Processor.

SMII

Micro Processor / Switch		MT2301
RXD0	←	SRXDAT0 (O)
TXD0	→	STXDAT0 (I)
TXCLK	→	STXCLK (I)
TXSYNC	→	STXSYNC (I)

Table 1.7: SMII Interface between MT2301 and Processor.

SS-SMII

Micro Processor / Switch		MT2301
RXD0	←	SRXDAT0 (O)
RXCLK	←	SRXCLK (O)
TXSYNC	←	SRXSYNC (O)
TXD0	→	STXDAT0 (I)
TXCLK	→	STXCLK (I)
TXSYNC	→	STXSYNC (I)

Table 1.8: SS-SMII Interface between MT2301 and Processor.

1.4 Boot Mode Selection

MT2301 supports SPI and HPI mode. The different boot settings are described below:

1.4.1 SPI Master Mode

Pin name	Description	Value when powering up
IRQ[A,B,C,D]	SPI mode	0000
EX_AA3	BIST	1
EX_A16	24 bit mode (Flash hold)	1
EX_A17	Do not care	X

Table 1.9: SPI Boot Mode Setup.

1.4.2 HPI Mode

Pin name	Description	Value when powering up
IRQ[A,B,C,D]	HPI mode	1110
EX_AA3	BIST	1
EX_A16	8 bit mode	0
EX_A17	Dual strobe	1

Table 1.10: HPI Boot Mode Setup.

1.5 Reset

Active low reset signal. To complete the reset function, the reset pin sequence of MT2301 must be slower than the sequence of 3.3V over 1ms.

※Note

When JTAG is not in use, the JTAG/OnCE test reset TRSTN (pin 94) should be short to system reset (pin 104) that shown as below.

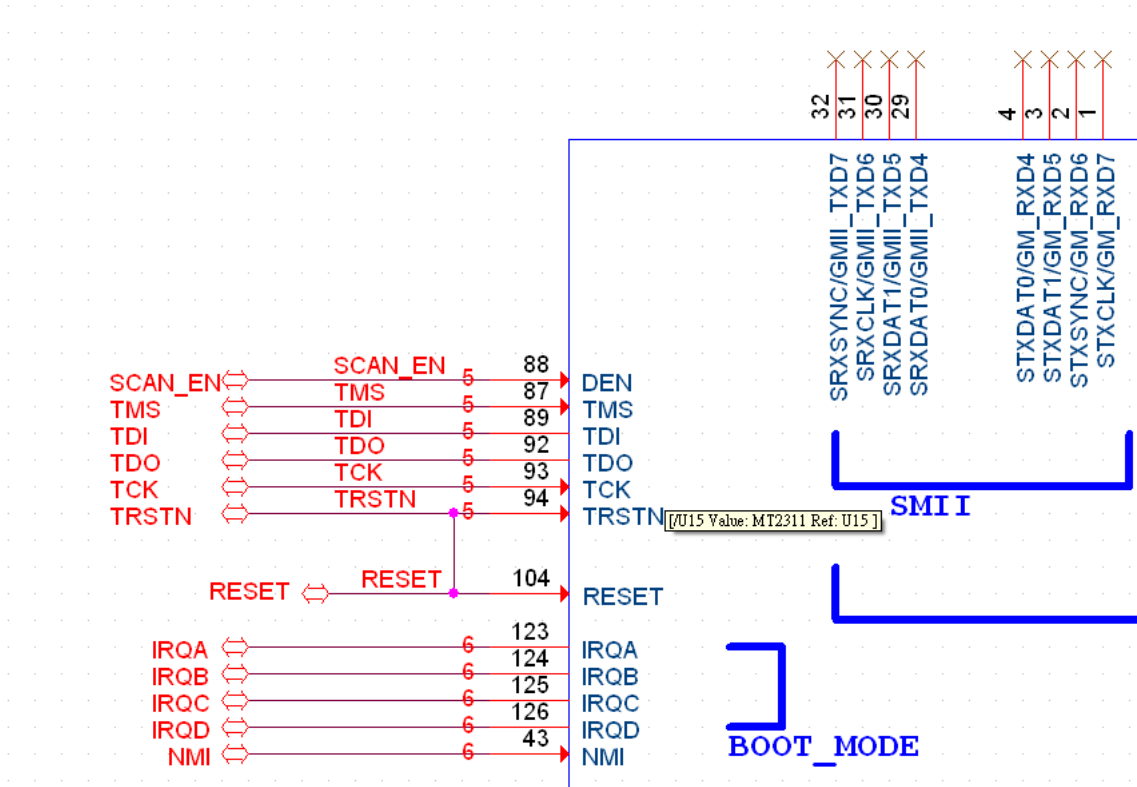


Figure 1.6: Reference Schematic for MT2301 Reset.

Shows the Power-on-Reset Timing Diagram as Below.

Symbol	Description	Min	Max	Unit	Remark
tD	Time between system reset and when 3.3V reaches 2V.	1	-	ms	

Table 1.11: Power on Sequence.

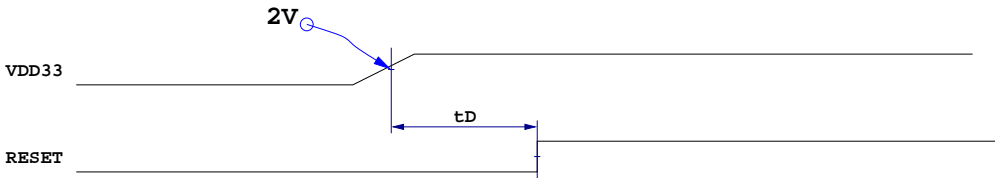
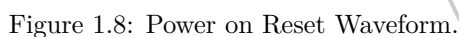


Figure 1.7: Reset Sequence.

Yellow:VDD33
Red:Reset Signal
Blue: VDD1.0



Chapter 2

MT2311

2.1 Power for MT2311

2.1.1 Power Consumption

Profile: 17a
 SNR: 6dB
 Side: CPE
 Mode: Interleave
 Transmission type: VDSL

	V	3.3V		1V	
Chip		Min	Max	Min	Max
MT2311		20	30	214	226

Table 2.1: MT2311 Power Consumption for 17a Profile Unit in mA.

Profile: 30a
 SNR: 6dB
 Side: CPE
 Mode: Interleave
 Transmission type: VDSL

	V	3.3V		1V	
Chip		Min	Max	Min	Max
MT2311		40	40	242	256

Table 2.2: MT2311 Power Consumption for 30a Profile Unit in mA.

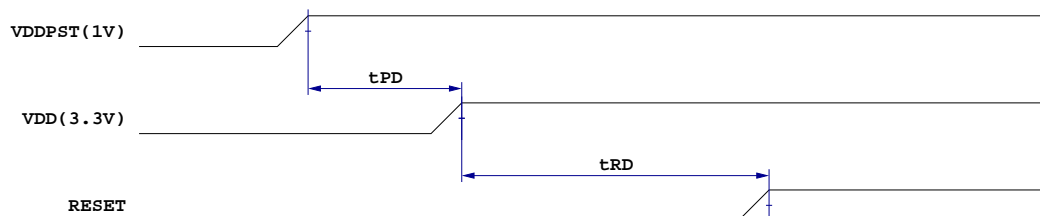
SNR: 6dB
 Side: CPE
 Mode: Fast
 Transmission type: ADSL2+/Ammex-L

	V	3.3V		1V	
Chip		Min	Max	Min	Max
MT2311		30	30	212	214

Table 2.3: MT2311 Power Consumption for ADSL2+/Ammex-L Unit in mA.

2.1.2 Power on Sequence

When powering up MT2311 the 3.3V power rail needs to be powered up first and then the 1V rail. The 3.3V does not need the power sequence request, but the sequence of 1V should be slower than the sequence of 3.3V over 200 μ S.



Symbol	Description	Min	Max	Unit	Remark
tPD	Time between digital core supply to digital I/O supply.	200	-	μ S	
tRD	Time between digital I/O supply to system reset.	200	-	μ S	

Table 2.4: Power on Sequence.

2.1.3 Power Noise

The power noise of each voltage should be below 75 mV.

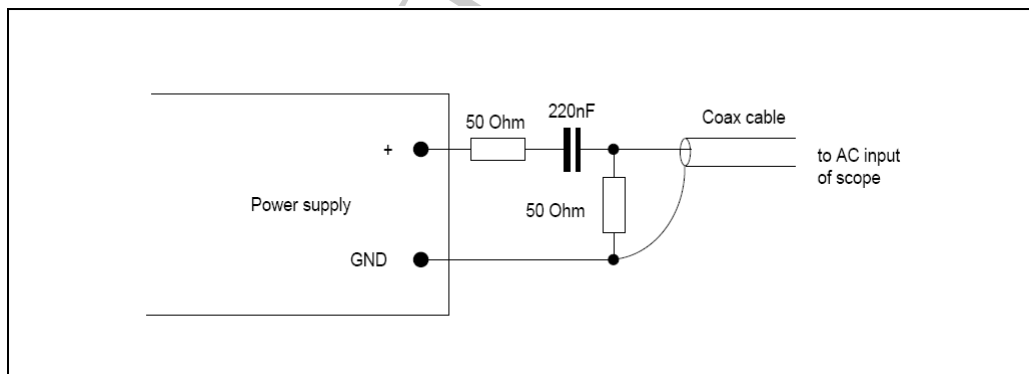


Figure 2.1: Preferred Method to Test Output Noise and Ripple.

2.2 System Clocks

Merlin chipset needs two system clocks for system operation, 25MHz clock is used for DMT and 35.328MHz is clock used for AFE.

2.2.1 System Clock for MT2311

The MT2311 need a 25MHz oscillator or external crystal resonator, two tuning capacitor and a 10K resistor is parallel with crystal as in reference schematic shown in Figure 2.2. The two tuning capacitors, C1 and C2 are corresponding to crystal loading capacitance, for example crystal specification loading capacitance use 18pF \pm 0.2pF/NPO dielectric. It is recommended to make sure the 25MHz jitter is smaller than 100 ps.

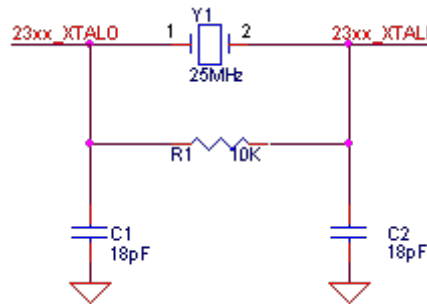


Figure 2.2: Reference Schematic for MT2311 Crystal.

2.3 Interfaces for MT2311

This section describes the MT2311 interfaces, including management interfaces (SPI/HPI/EBM) and data interfaces (MII/SMII/GMII/RGMII). Each of the data interface output pins has an internal 40 ohm resistor.

2.3.1 SPI

The Serial Peripheral Interface (SPI) is a synchronous serial data link, that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

SPI flash		MT2311
CS_n	←	SC2B(pin 84)
SCK	←	SCKB(pin 81)
SI	←	STDB(pin 82)
SO	→	SRDB(pin 83)

Table 2.5: SPI Master Boot.

Micro Processor		MT2311
CS_n	→	SC2C/EX_D3/11(pin 116)
SCK	→	SCKC/EX_D0/8(pin 111)
SI	←	STDC/EX_D2/10(pin 113)
SO	→	SRDC/EX_D1/9(pin 112)

Table 2.6: SPI Slave Boot.

2.3.2 HPI

HPI bus (Host Port Interface bus) is a flexible interface that enables a micro processor to use the interface to load firmware and manage the MT2311. Through the HPI bus a micro processor can access VDSL MIBs and there through get/set VDSL status.

Micro Processor		MT2311
CPU_CS_n	→	HP_CS (pin 108)
CPU_OE_n	→	HP_RD (pin 109)
CPU_WE_n	→	HP_DS (pin 110)
Data_7	↔	EX_D7/15 (pin 122)
Data_6	↔	EX_D6/14 (pin 121)
Data_5	↔	EX_D5/13 (pin 118)
Data_4	↔	EX_D4/12 (pin 117)
Data_3	↔	SC2C/EX_D3/11 (pin 116)
Data_2	↔	STDC/EX_D2/10 (pin 113)
Data_1	↔	SRDC/EX_D1/9 (pin 112)
Data_0	↔	SCKC/EX_D0/8 (pin 111)

Table 2.7: Interface between MT2311 and Processor.

HPI Debugging Step by Step

If implementing control by using HPI and some problems are encountered, the suggested method to debug HPI bus step by step is the following:

- Set MT2311 boot mode:
 - Set to boot from SPI flash, IRQ[A,B,C,D] to: '0000'.
 - MT2311 pin 96 change 10k resistor voltage to 3.3V.
 - Load test firmware to SPI flash use the Eyebox tool to burn firmware "HPI_TEST_010201_121109_144714".
- Access MCU with HPI and do Read/Write testing, each read and write are 8 bytes, timing and sequence are like the following:
 - First of all write the following 8 bytes to the HPI: 00 6c 31 00 00 00 45 71 (no need for extra delay between each byte). Wait 500 μ s, then read 8 bytes back from HPI, if the read action succeeds, the content of the data should be like this: 00 6c 31 01 01 00 41 32 (no need for extra delay between each byte).
 - Those 8 bytes we write into HPI can be verified by using DslMonitor application, open DslMonitor, Monitor variable "HostRxCmdFifo" as in Figure 2.3:

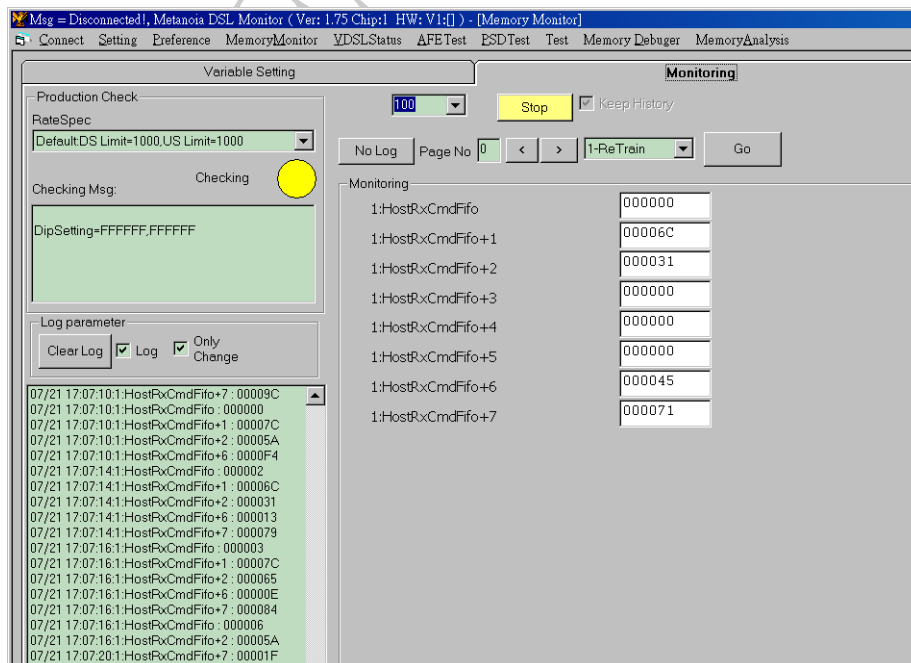


Figure 2.3: HPI Debug Interface.

Boot from HPI Interface

1. Reset MT2311 for 5ms.
2. Wait 1000ms for BIST to be completed.
3. Load firmware, byte interleave recommended to be $>8\mu\text{s}$.
4. Load firmware complete and wait 100ms.
5. Write 8 byte data without inter-byte gap.
6. Wait $300\mu\text{s}$.
7. Read 8 byte data with inter-byte gap $>8\mu\text{s}$.
8. Wait $300\mu\text{s}$.
9. Repeat item 5 to 8 for read/write data.

2.3.3 Ethernet Interfaces

The Media Independent Interface(MII, SMII, GMII, RGMII) provides Ethernet connectivity between 10/100/1000 Media Access Control (MAC) and Physical Layer (PHY) devices. MT2311 uses MII in PHY mode and the following figures show how to connect the xMII interface with a network processor.

MII (PHY Mode)

Micro Processor / Switch		MT2311
RXDV	←	MII_RXDV(O)
RXCLK	←	MII_RXCLK(O)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
COL	←	MII_COL(O)
CRS	←	MII_CRS(O)
TXEN	→	MII_TXEN(I)
TXCLK	←	MII_TXCLK(O)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)

Table 2.8: MII (PHY Mode) Interface between MT2311 and Processor.

MII (MAC Mode)

Micro Processor / Switch		MT2311
RXDV	←	MII_RXDV(O)
RXCLK	→	MII_RXCLK(I)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
COL	←	MII_COL(O)
CRS	←	MII_CRS(O)
TXEN	→	MII_TXEN(I)
TXCLK	→	MII_TXCLK(I)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)

Table 2.9: MII (MAC Mode) Interface between MT2311 and Processor.

SMII

Micro Processor / Switch		MT2311
RXD0	←	SRXDAT0 (O)
TXD0	→	STXDAT0 (I)
TXCLK	→	STXCLK (I)
TXSYNC	→	STXSYNC (I)

Table 2.10: SMII Interface between MT2311 and Processor.

SS-SMII

Micro Processor / Switch		MT2311
RXD0	←	SRXDAT0 (O)
RXCLK	←	SRXCLK (O)
TXSYNC	←	SRXSYNC (O)
TXD0	→	STXDAT0 (I)
TXCLK	→	STXCLK (I)
TXSYNC	→	STXSYNC (I)

Table 2.11: SS-SMII Interface between MT2311 and Processor.

GMII

Micro Processor / Switch		MT2311
RXCTL	←	MII_RXDV(O)
RXCLK	←	MII_RXCLK(O)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
RXD4	←	MII_RXD4(O)
RXD5	←	MII_RXD5(O)
RXD6	←	MII_RXD6(O)
RXD7	←	MII_RXD7(O)
TXCTL	→	MII_TXEN(I)
TXCLK	→	MII_TXCLK(I)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)
TXD4	→	MII_TXD4(I)
TXD5	→	MII_TXD5(I)
TXD6	→	MII_TXD6(I)
TXD7	→	MII_TXD7(I)

Table 2.12: GMII Interface between MT2311 and Processor.

RGMII

Micro Processor / Switch		MT2311
RXCTL	←	MII_RXDV(O)
RXCLK	←	MII_RXCLK(O)
RXD0	←	MII_RXD0(O)
RXD1	←	MII_RXD1(O)
RXD2	←	MII_RXD2(O)
RXD3	←	MII_RXD3(O)
TXCTL	→	MII_TXEN(I)
TXCLK	→	MII_TXCLK(I)
TXD0	→	MII_TXD0(I)
TXD1	→	MII_TXD1(I)
TXD2	→	MII_TXD2(I)
TXD3	→	MII_TXD3(I)

Table 2.13: RGMII Interface between MT2311 and Processor.

2.4 Boot Mode Selection

MT2311 supports SPI/HPI/Slave SPI/EBM mode. The different boot settings are described below:

2.4.1 SPI Master Mode

Pin name	Description	Value when powering up
IRQ[A,B,C,D]	SPI mode	0000
EX_AA3	BIST	1
EX_A16	24 bit mode (Flash hold)	1
EX_A17	Single strobe (no use)	0

Table 2.14: SPI Boot Mode Setup.

2.4.2 HPI Mode

Pin name	Description	Value when powering up
IRQ[A,B,C,D]	HPI mode	1110
EX_AA3	BIST	1
EX_A16	8 bit mode	0
EX_A17	Dual strobe	1

Table 2.15: HPI Boot Mode Setup.

2.4.3 SPI Slave Mode

Use port C enable, see reference circuit to enable port C.

Pin name	Description	Value when powering up
IRQ[A,B,C,D]	Slave SPI mode	0010
EX_AA3	BIST	1
EX_A16	Do not care.	X
EX_A17	SPI slave enable	1

Table 2.16: HPI Boot Mode Setup.

Pin name	Description
SCKC/EX_D0/8 (Pin 111)	SCKC
SRDC/EX_D1/9 (Pin 112)	SRDC
STDC/EX_D2/10 (Pin 113)	STDC
SC2C/EX_D3/11 (Pin 116)	SC2C

Table 2.17: Port C Setup.

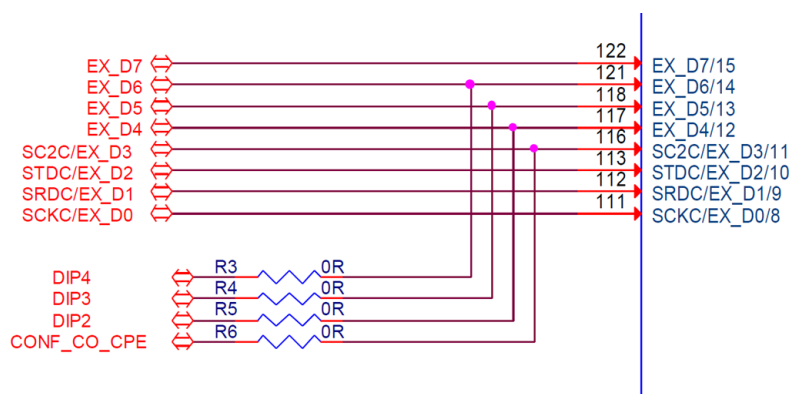


Figure 2.4: Hardware Circuit to Run Slave SPI Mode.

2.4.4 EBM Mode

Pin name	Description	Value
IRQ[A,B,C,D]	EBM mode	0101
EX_AA3	BIST	1

Pin name	MII mode	SMII mode	RGMII mode	GMII mode
EX_A16	1	0	1	0
EX_A17	0	0	1	1

Table 2.18: EBM Boot Mode Setup.

2.5 Reset

Active low reset signal. To complete the reset function, the reset pin sequence of MT2311 must be slower than the sequence of 3.3V over 1ms. After reset, about 30ms is needed for the MT2311 to startup and initialization.

※Note

When JTAG is not in use, the JTAG/OnCE test reset TRSTN (pin 94) should be short to system reset (pin 104) that shown as below.

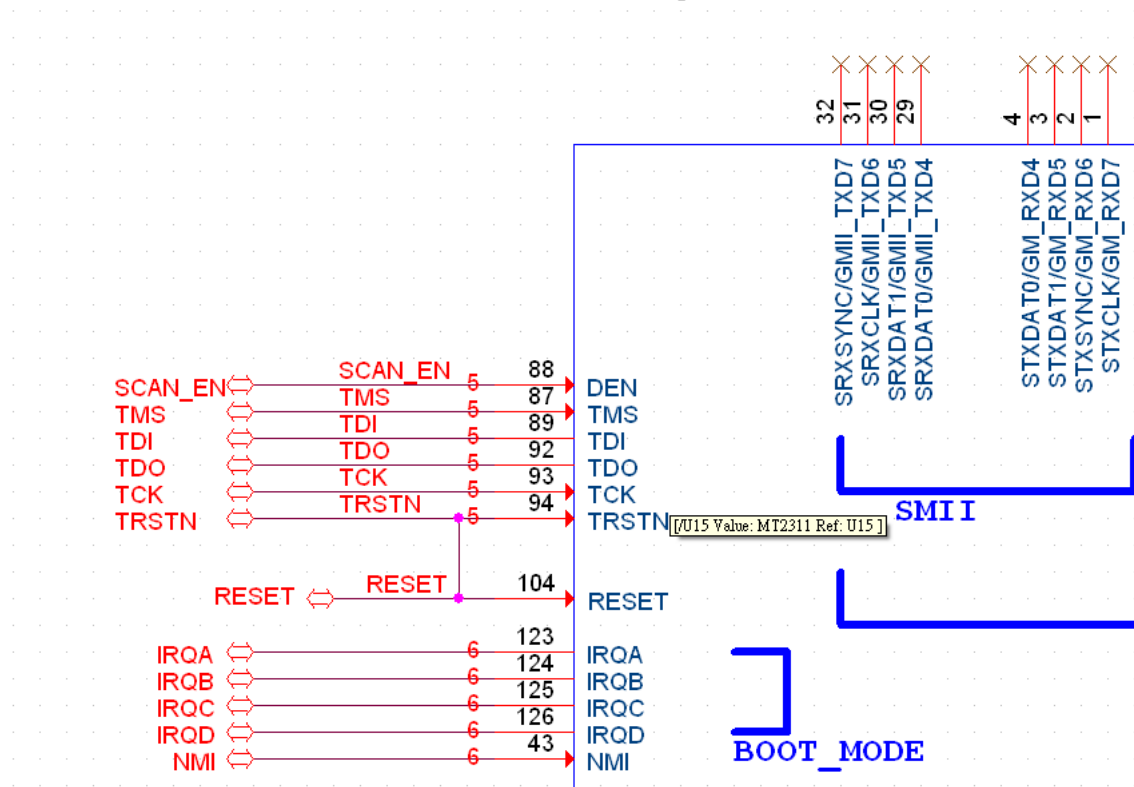


Figure 2.5: Reference Schematic for MT2311 Reset.

Shows the Power-on-Reset Timing Diagram as Below.

Symbol	Description	Min	Max	Unit	Remark
tD	Time between system reset and when 3.3V reaches 2V.	1	-	ms	

Table 2.19: Power on Sequence.

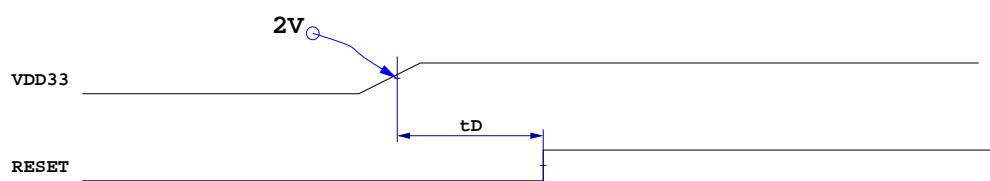


Figure 2.6: Reset Sequence.

Yellow: VDD33
Red: Reset Signal
Blue: VDD1.0

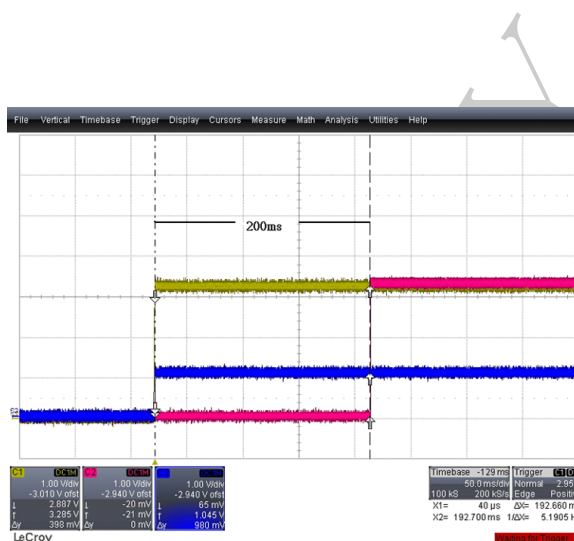


Figure 2.7: Power on Reset Waveform.

Chapter 3

MT3301

3.1 Power for MT3301

3.1.1 Power Consumption

Profile: 17a
 SNR: 6dB
 Side: CPE
 Mode: Interleave

	V	5V		3.3V		2.5V	
Chip		Min	Max	Min	Max	Min	Max
MT3301		155	197	20	30	194	224

Table 3.1: MT3301 Power Consumption for 17a Profile Unit in mA.

Profile: 30a
 SNR: 6dB
 Side: CPE
 Mode: Interleave

	V	5V		3.3V		2.5V	
Chip		Min	Max	Min	Max	Min	Max
MT3301		177	202	40	40	264	291

Table 3.2: MT3301 Power Consumption for 30a Profile Unit in mA.

3.1.2 Power on Sequence

MT3301:No power on sequence requirement.

3.1.3 Power Noise

The power noise of each voltage should be below 75 mV.

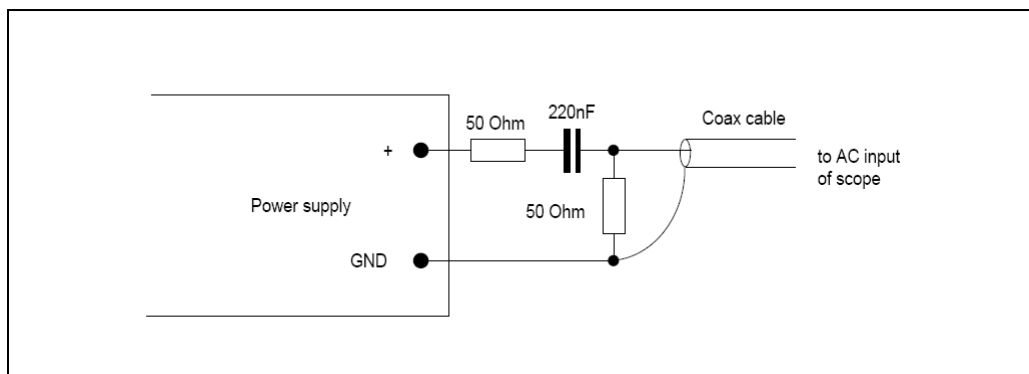


Figure 3.1: Preferred Method to Test Output Noise and Ripple.

3.2 System Clocks

Merlin chipset needs two system clocks for system operation, 25MHz clock is used for DMT and 35.328MHz is clock used for AFE.

3.2.1 System Clock for MT3301

MT3301 set in CPE mode

When working in CPE mode, the 35.328MHz crystal resonator with ± 200 ppm pullability function is required, the AFE's internal capacitors within a range from 6pF to 38pF in about 5fF-steps at both XTAL1/2 pins. The resulting pullability on the crystal are ± 200 ppm frequency range. Figure 2.2 shows CL1/CL2 are internal variable capacitors in series with the crystal to accomplished pullability function.

MT3301 set in CO mode

When working in CO mode, it is recommended use oscillator to supply 35.328MHz(± 30 ppm) clock input to 330x_XTAL1 pin and to integrat the phase noise form 12KHz to 5MHz that calculated the jitter should be under 0.3ps. It also can use the same crystal as in CO mode, CL1 and CL2 should be fixed at 18pF which resulting in a fixed clock at 35.328MHz.

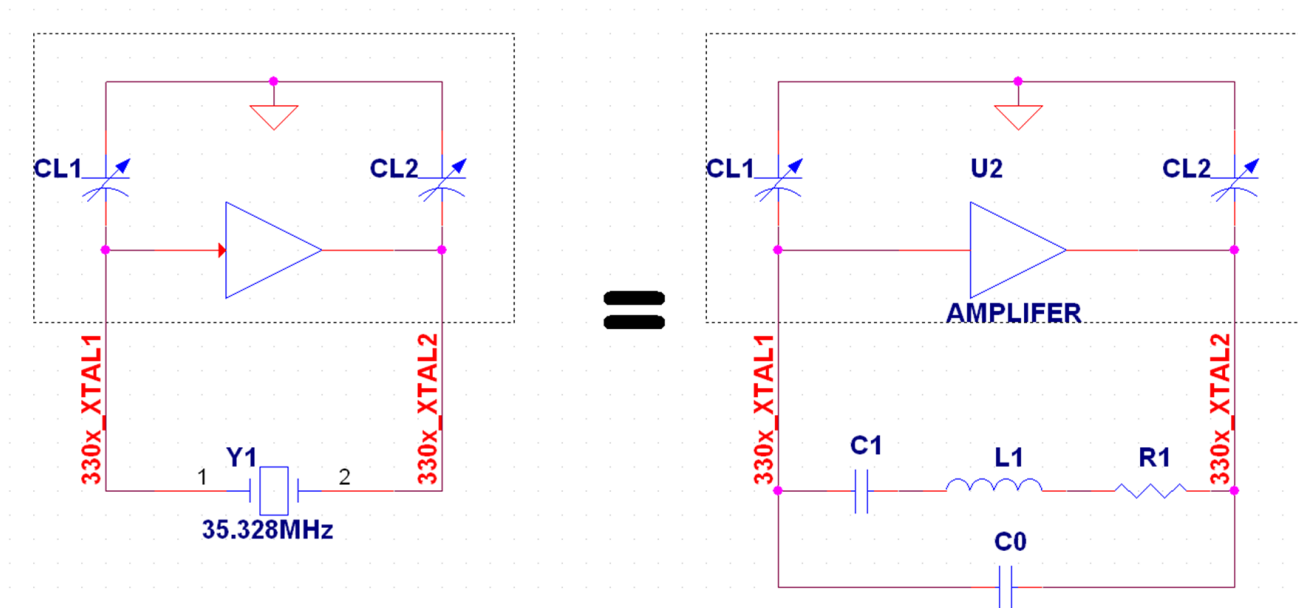


Figure 3.2: Reference Schematic for MT3301 35.328MHz Crystal.

Pullability can be expressed in ppm as: $\frac{F_L - F_S}{F_S} = \frac{\Delta F}{F_S} = \frac{C_1}{2(C_0 - C_L)}$

3.3 Hybrid Layout for MT3301

In this section a number of important notes on the design of the hybrid schematic are listed. It is important to follow these guidelines to ensure good performance for the xDSL.

- Differential pair HYBINP/HYBINN, OUT_P1/OUT_N1, OUT_P2/OUT_N2 layout trace gap should be under **6mil**.
- Differential pair HYBINP/HYBINN, OUT_P1/OUT_N1, OUT_P2/OUT_N2 layout trace width should be over **12mil** (If layout have extra space , suggest the trace width to use 20mil).
- Differential pair should be enclosed with ground plane and of the same length.

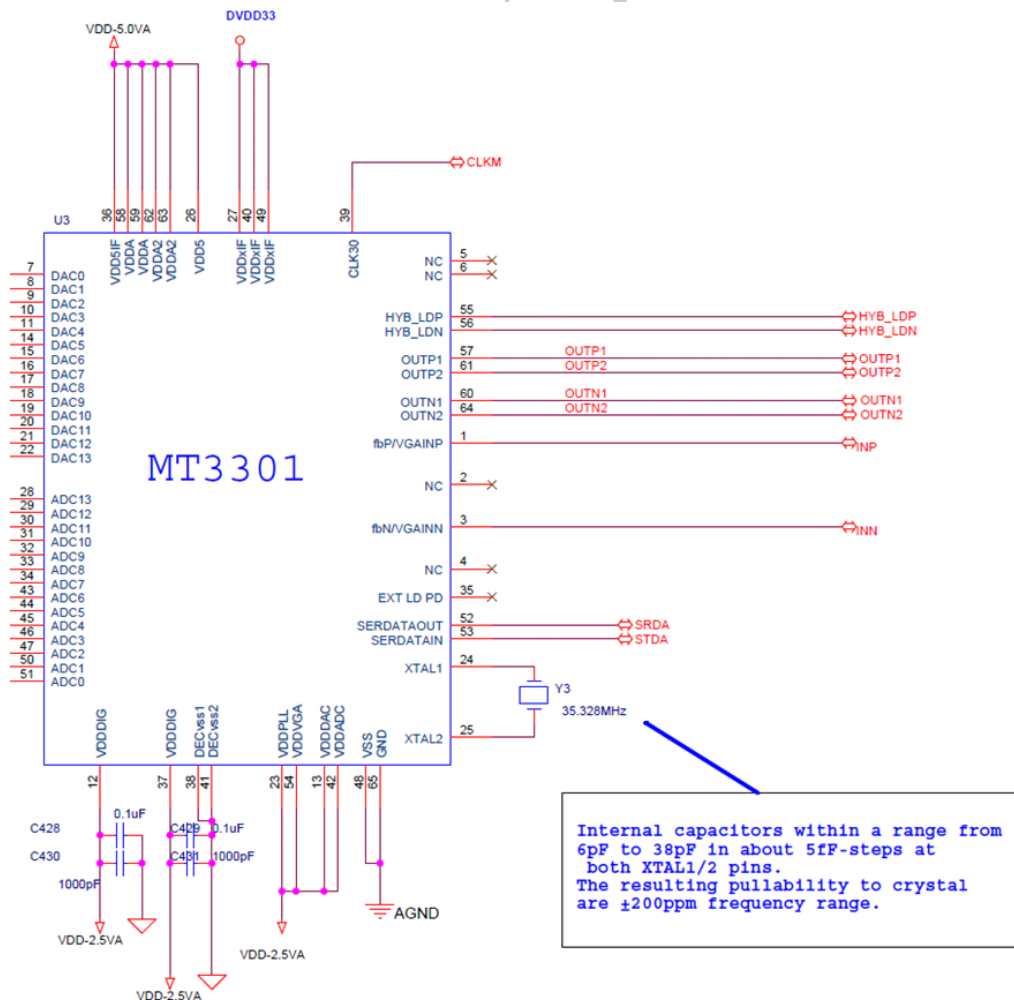
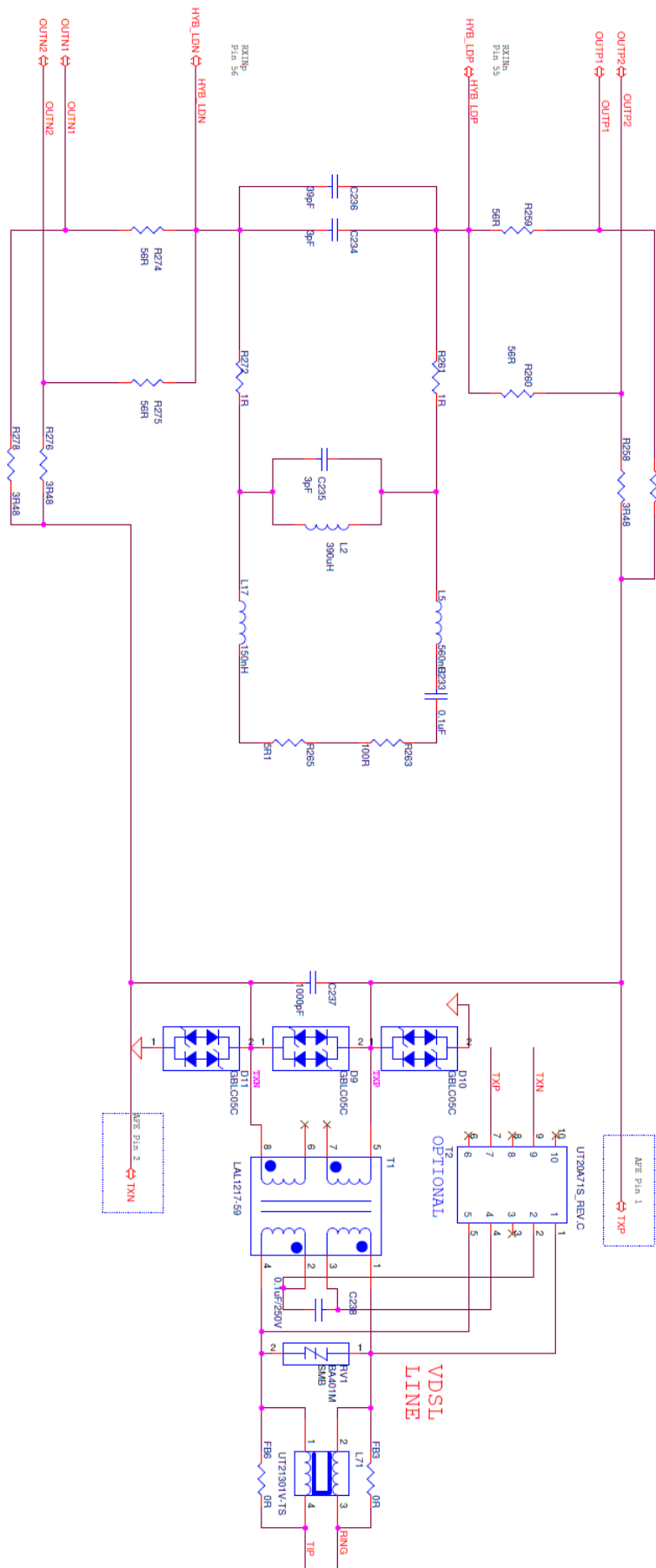


Figure 3.3: MT3301 Pinout Schematic.



3.3.1 Line Driver Output Component Placement

- Components R257,R278,R258,R276,C237 should be placed close to transformer(T1).
- Resistors R257,R278 should be placed in the top layer, R258,R276 place on bottom layer as shown in Figure 3.5.
- Hybrid schematic and line driver circuit must be covered by ground plane as shown in Figure 3.6 and 3.7 (the gap between circuit and ground plane should be under 12 mil).

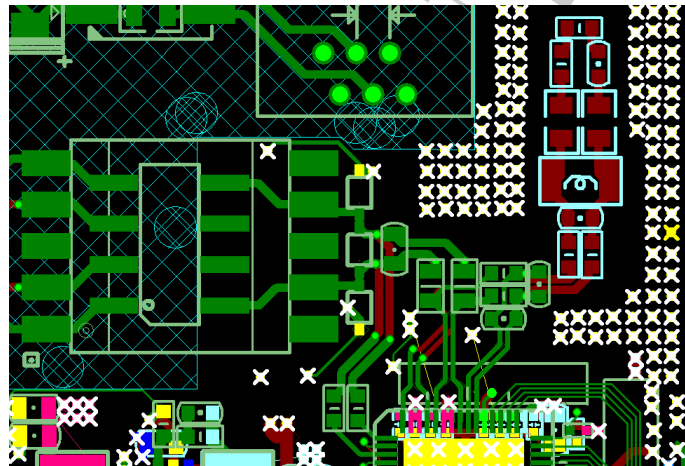


Figure 3.5: Line Driver Top and Bottom Layer Layout.

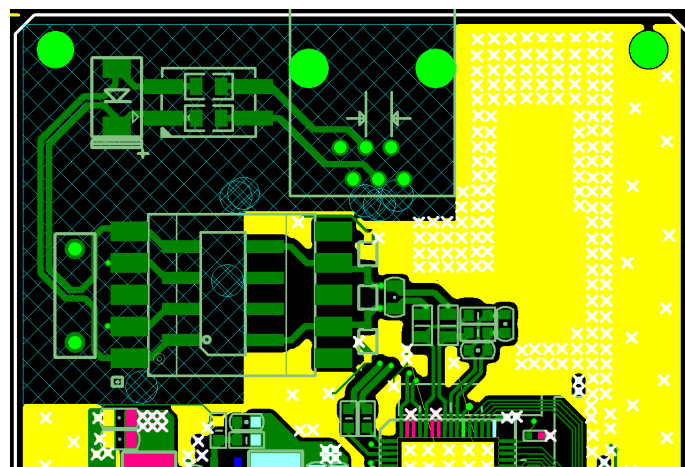


Figure 3.6: Line Driver Top Layer Layout.

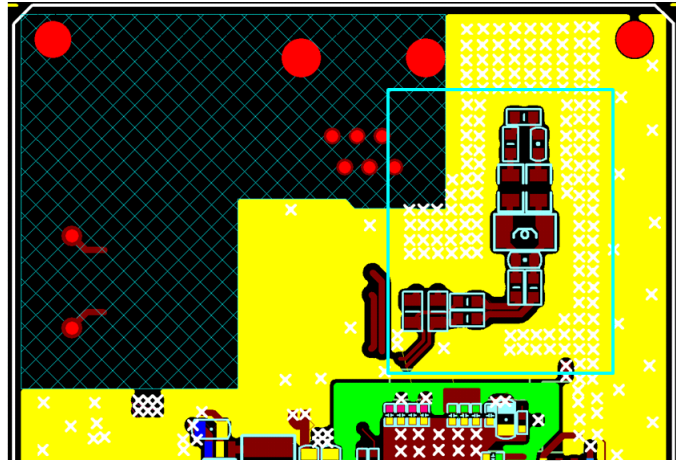


Figure 3.7: Line Driver Bottom Layer Layout.

External Hybrid Component Placement

- Hybrid components R259,R274 place near R257,R278 on top layer.
- Hybrid components R260,R275 place near R258,R276 on bottom layer.
- R260,R275,R261,R272,L2,C235,L12,L15,L3,L4,C233,R263,L1,R265,R270 place on bottom layer as shown in Figure 3.7.

MT3301 Input Routing Trace

- The pin 1 and pin 3 of MT3301 are connected to the transformer(T1), and the gap between these two trances should be under 6mil and enclose with ground plane.

Transformer and DC Block Capacitor

- The trace width needs to be 20mil or above and need shortest routing, as show in Figure 3.6.

2.5V Power Plane

- It is recommended to put the 2.5V power plane in the bottom layer and circle with AFE GND pad consistently, as shown in Figure 3.8.



Figure 3.8: 2.5V Plane (Green Plane) of Bottom Layer.

5V Power Plane

- It is recommended to put the 5V power plane in layer 3 and circle with AFE GND pad consistently, as shown in Figure 3.9.

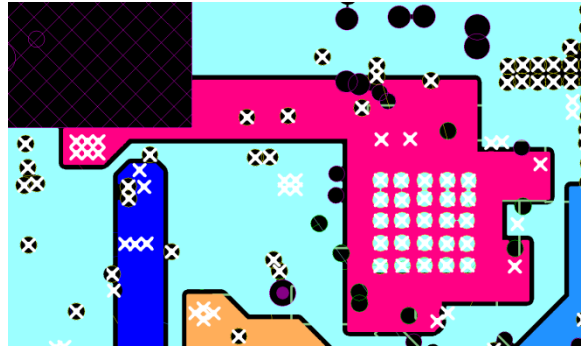


Figure 3.9: 5V Plane (Pink Plane) of Layer 3.

3.3V Power Plane

- 3.3V power does not need power plane but the trace should be at least 12 ~ 20mil where it connectors with the 3.3V power source.

TIP and RING Race

- It is recommended that TIP and RING traces use parallel trace and for certification issue both trace need keep 3mm distance from main board GND plane or other digital traces.

Bypass Capacitor

- It is recommended to follow the layout topology for MT3301 pin 37,38,41 and 42 as in Figure 3.10.
- For MT3301 pin 58,59,62 and 63 it is recommended to follow the layout topology as shown in Figure 3.11.

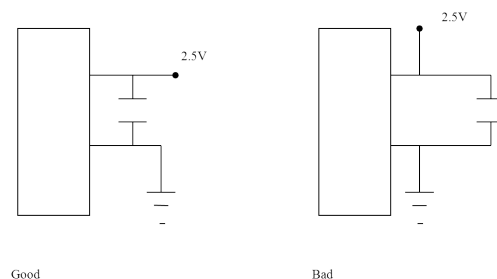


Figure 3.10: Layout for Pin 37,38,41 and 42.

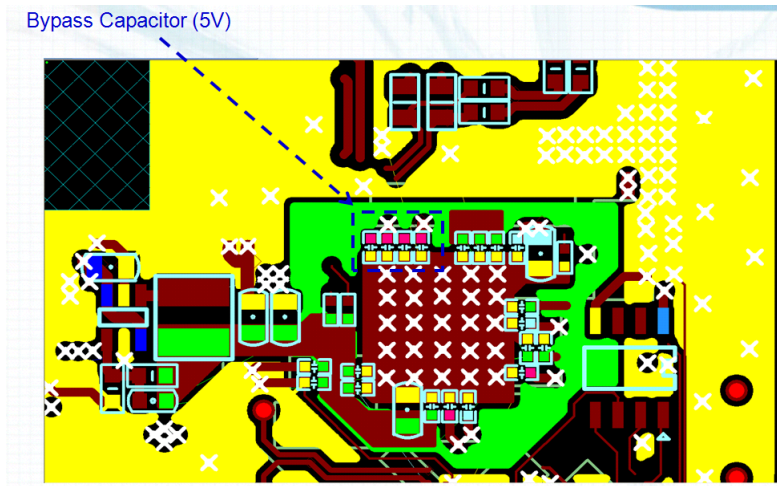


Figure 3.11: Layout for Bypass Capacitor.

Chapter 4

MT3302

4.1 Power for MT3302

4.1.1 Power Consumption

Profile: 17a
 SNR: 6dB
 Side: CPE
 Mode: Interleave
 Transmission type: VDSL

Chip \ V	5V		3.3V		2.5V	
	Min	Max	Min	Max	Min	Max
MT3302	162	202	20	30	212	240

Table 4.1: MT3302 Power Consumption for 17a Profile Unit in mA.

Profile: 30a
 SNR: 6dB
 Side: CPE
 Mode: Interleave
 Transmission type: VDSL

Chip \ V	5V		3.3V		2.5V	
	Min	Max	Min	Max	Min	Max
MT3301	177	202	40	40	282	321

Table 4.2: MT3302 Power Consumption for 30a Profile Unit in mA.

SNR: 6dB
 Side: CPE
 Mode: Fast
 Transmission type: ADSL2+/Ammex-L

Chip \ V	5V		3.3V		2.5V	
	Min	Max	Min	Max	Min	Max
MT3302	170	214	30	30	182	239

Table 4.3: MT3302 Power Consumption for ADSL2+/Ammex-L Unit in mA.

4.1.2 Power on Sequence

MT3302 :No power on sequence requirement.

4.1.3 Power Noise

The power noise of each voltage should be below 75 mV.

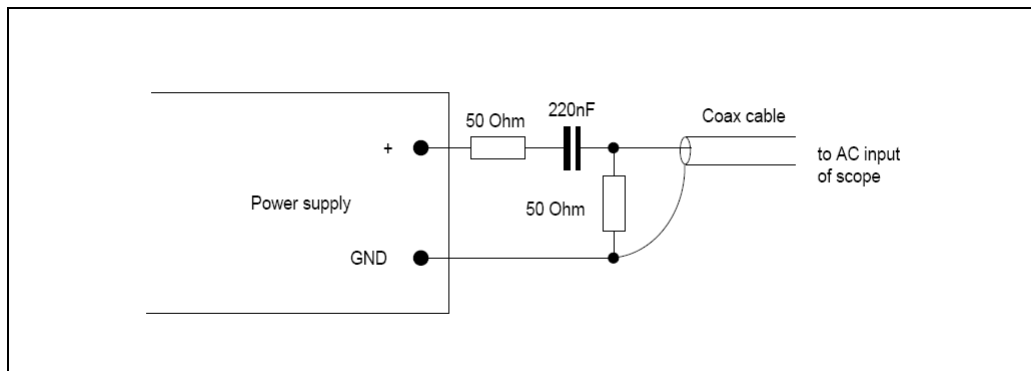


Figure 4.1: Preferred Method to Test Output Noise and Ripple.

4.2 System Clocks

Merlin chipset needs two system clocks for system operation, 25MHz clock is used for DMT and 35.328MHz is clock used for AFE.

4.2.1 System Clock for MT3302

MT3302 set in CPE mode

When working in CPE mode, the 35.328MHz crystal resonator with ± 200 ppm pullability function is required, the AFE's internal capacitors within a range from 6pF to 38pF in about 5fF-steps at both XTAL1/2 pins. The resulting pullability on the crystal are ± 200 ppm frequency range. Figure 4.2 shows CL1/CL2 are internal variable capacitors in series with the crystal to accomplished pullability function.

MT3302 set in CO mode

When working in CO mode, it is recommended use oscillator to supply 35.328MHz(± 30 ppm) clock input to 330x_XTAL1 pin and to integrat the phase noise form 12KHz to 5MHz that calculated the jitter should be under 0.3ps. It also can use the same crystal as in CO mode, CL1 and CL2 should be fixed at 18pF which resulting in a fixed clock at 35.328MHz.

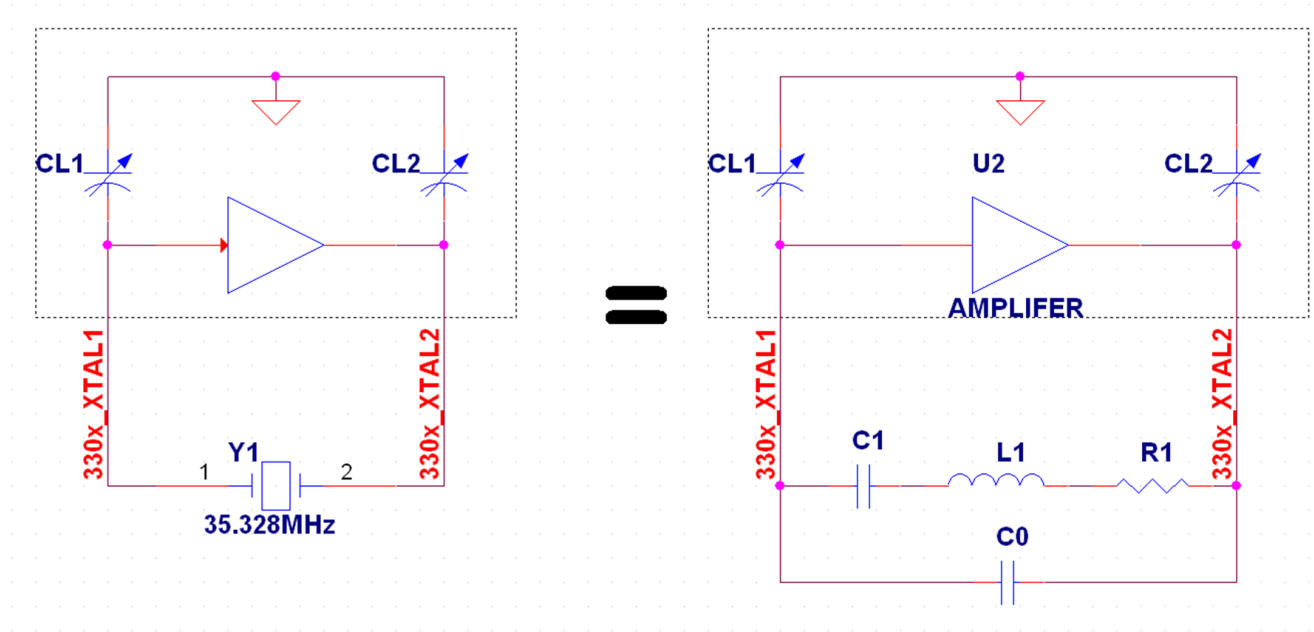


Figure 4.2: Reference Schematic for MT3302 35.328MHz Crystal.

Pullability can be expressed in ppm as: $\frac{F_L - F_S}{F_S} = \frac{\Delta F}{F_S} = \frac{C_1}{2(C_0 - C_L)}$

4.3 Hybrid Layout for MT3302

In this section a number of important notes on the design of the hybrid schematic are listed. It is important to follow these guidelines to ensure good performance for the xDSL.

- Differential pair VGAINP/VGAINN,VGAINPATT/VGAINNATT,OUT_P1/OUT_N1,OUT_P2/OUT_N2 layout trace gap should be under **20mil**.
- Differential pair VGAINP/VGAINN,VGAINPATT/VGAINNATT,OUT_P1/OUT_N1,OUT_P2/OUT_N2 layout trace width should be under **20mil**.
- Differential pair should be enclosed with ground plane and of the same length.
- The gap between the trace and ground should be the same as the trace width.

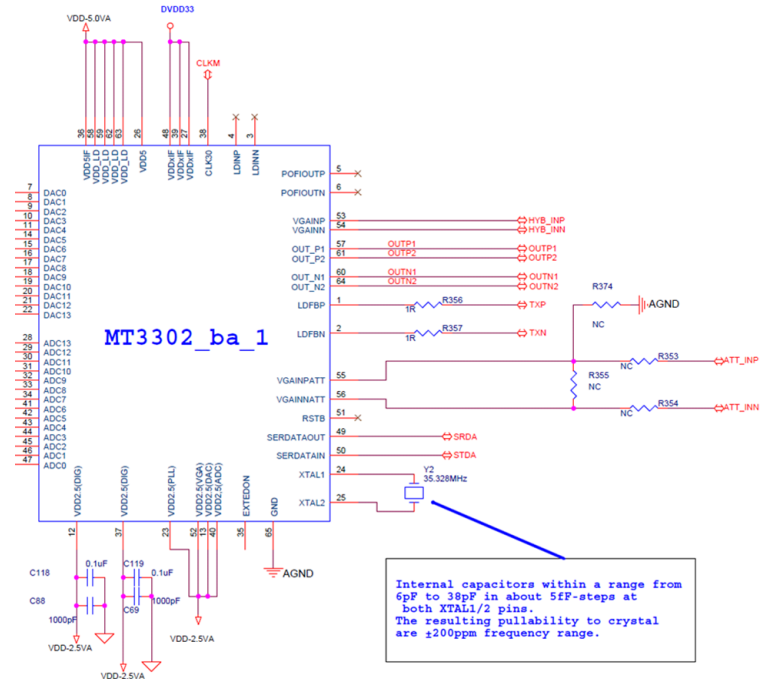


Figure 4.3: MT3302 Pinout Schematic.

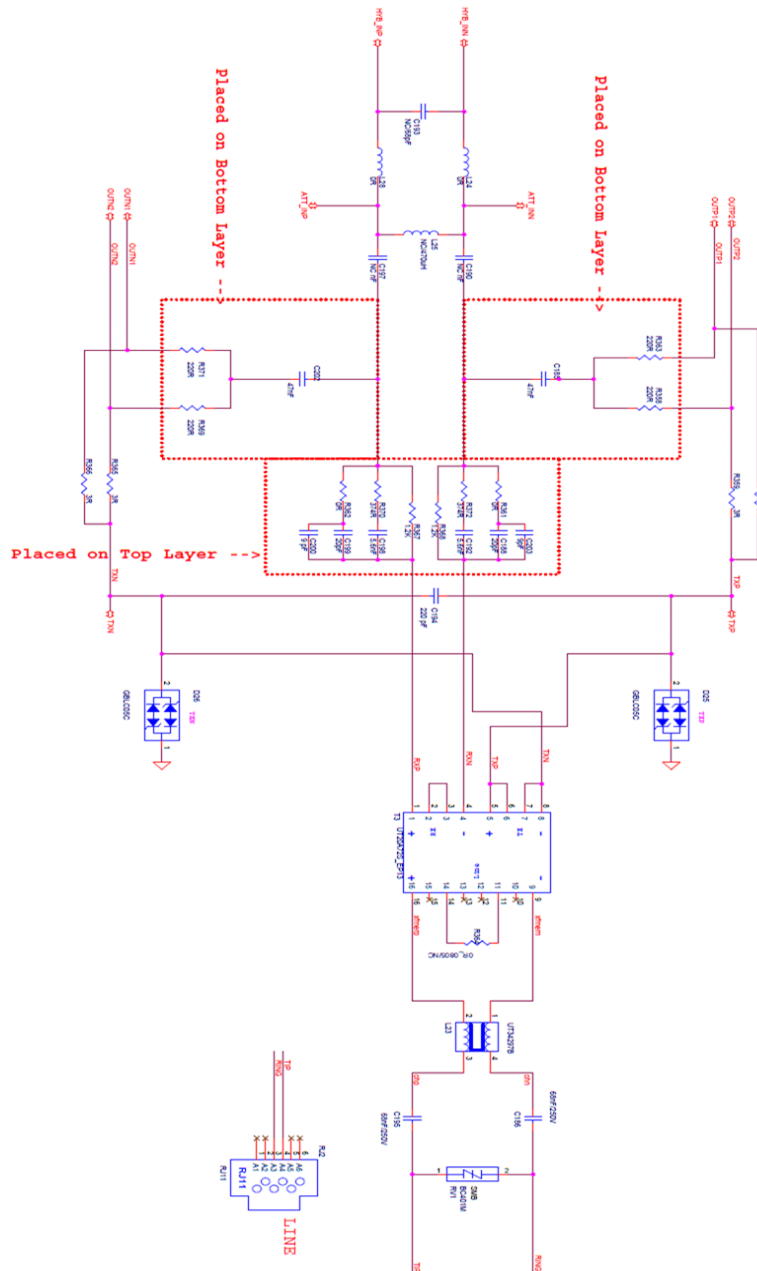


Figure 4.4: MT3302 Hybrid Schematic.

4.3.1 Line Driver Output Component Placement

- Components R359,R360,R365,R366,R363,R358,R369,R371,C194 should be placed close to transformer(T3).
- Resistors R359,R360,R365,R366,R363,R358,R369,R371,C194 should be placed in the bottom layer as shown in Figure 4.5.
- Hybrid schematic and line driver circuit must be covered by ground plane as shown in Figure 4.6 (the gap between circuit and ground plane should be under 20 mil).



- Hybrid components R361,R362,R368,R367,R370,R372,C188,C192,C198,C190,C197,L25,L24,L28,C193 should be placed close to transformer(T3).
- Hybrid components R361,R362,R368,R367,R370,R372,C188,C192,C198,C190,C197,L25,L24,L28,C193 should be placed in the top layer as shown in Figure 4.7.

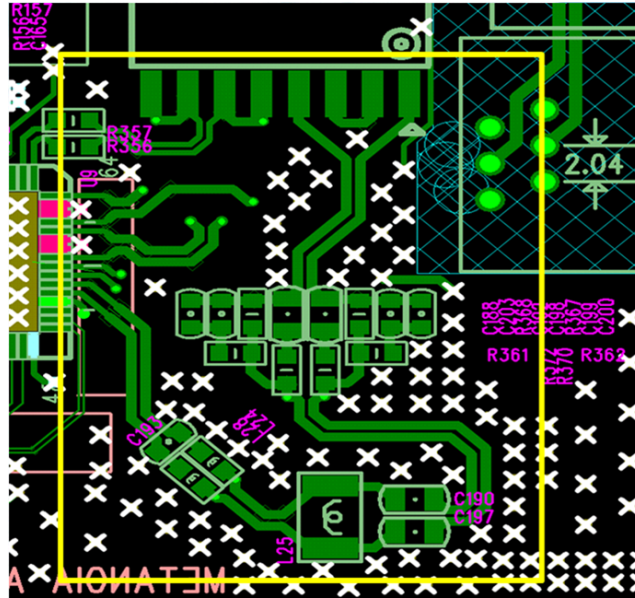


Figure 4.7: Components Placement.

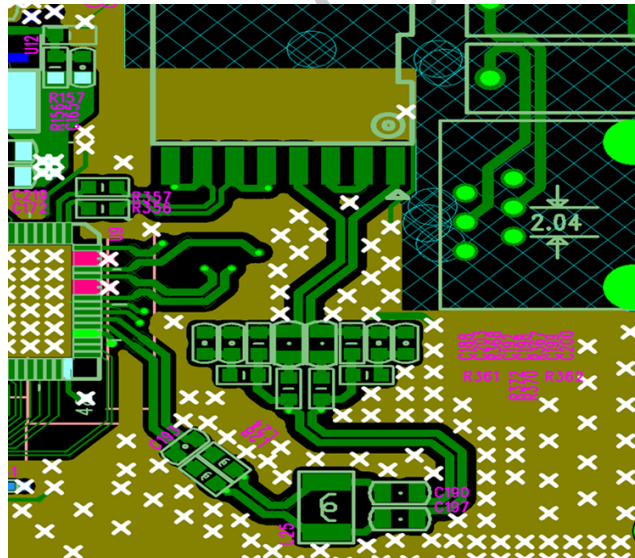


Figure 4.8: Hybrid Top Layer Layout.

MT3302 Internal LD FeedBack Input Trace

- Pin no.1 and 3 of MT3302 should be connected to the transformer(T3), the layout trace width should be under **12mil** and the gap between the trace and ground plane should be under **12 mil** as shown in Figure 4.9.

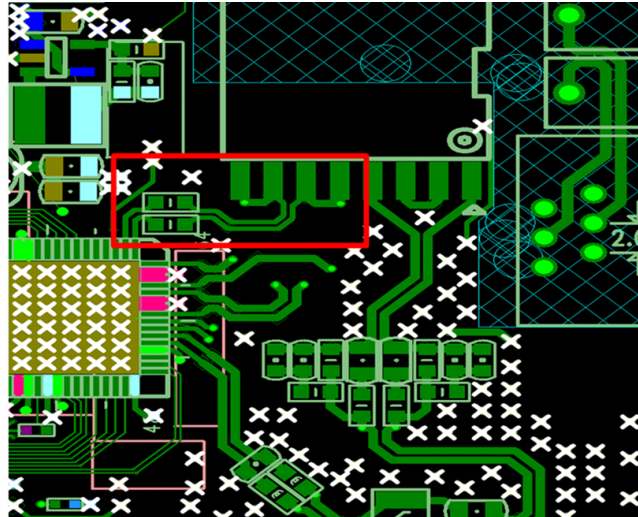


Figure 4.9: Feedback Trace Routing between Transformer and MT3302.

Transformer and DC Block Capacitor

- The trace width needs to be 20mil or above and need shortest routing, as show in Figure 4.10.

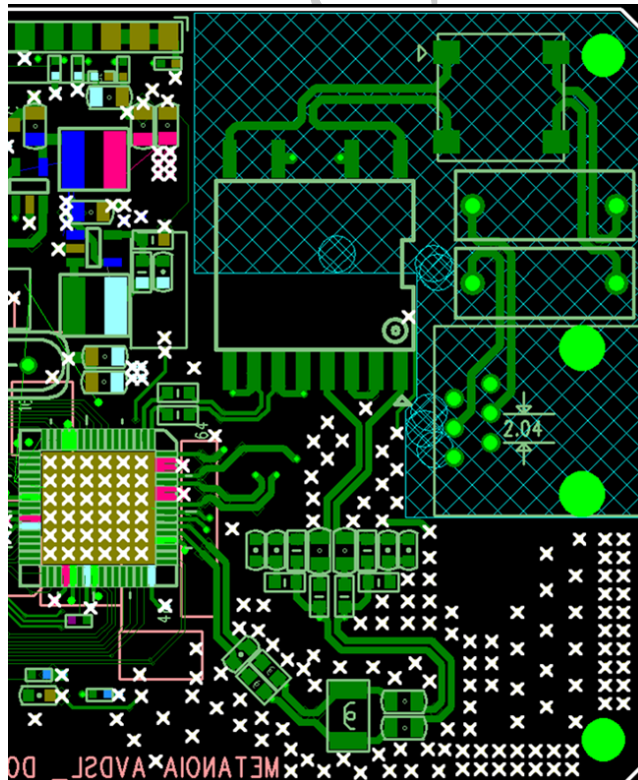


Figure 4.10: Trandformer and DC Block Capacitor Placement.

2.5V Power Plane

- It is recommended to put the 2.5V power plane in the bottom layer and circle with AFE GND pad consistently, as shown in Figure 4.11.



Figure 4.11: 2.5V Plane (Green Plane) of Bottom Layer.

5V Power Plane

- It is recommended to put the 5V power plane in layer 3 and circle with AFE GND pad consistently, as shown in Figure 4.12.

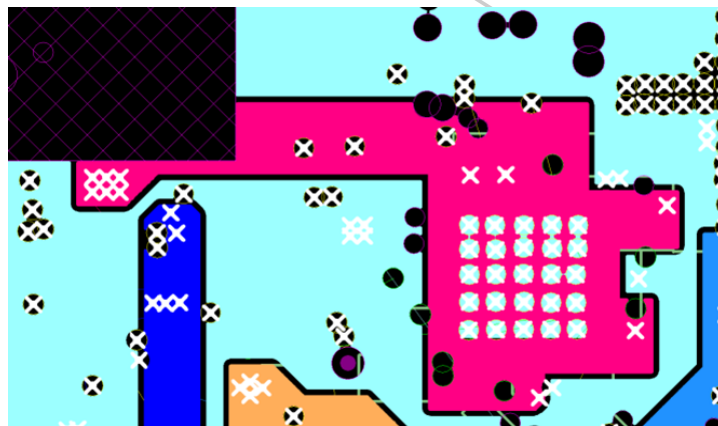


Figure 4.12: 5V Plane (Pink Plane) of Layer 3.

3.3V Power Plane

- 3.3V power does not need power plane but the trace should be at least 12 ~ 20mil where it connects with the 3.3V power source.

TIP and RING Trace

- It is recommended that TIP and RING traces use parallel trace and for certification issue both trace need keep 3mm distance from main board GND plane or other digital traces.

Bypass Capacitor

- It is recommended to follow the layout topology for MT3302 pin 37, 12, 40 and 52 as in Figure 4.13.
- For MT3302 pin 58, 59, 62 and 63 it is recommended to follow the layout topology as shown in Figure 4.14.

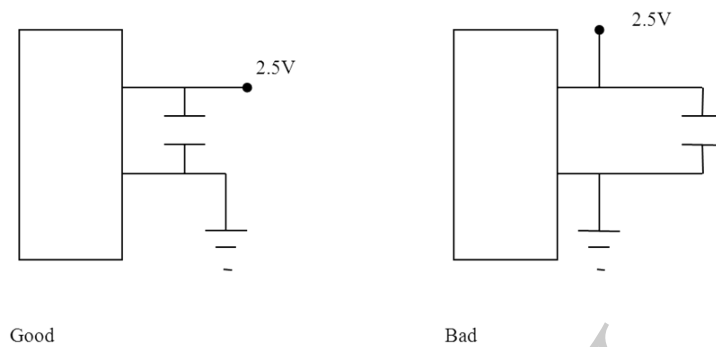


Figure 4.13: Layout for MT3302 Pin 12, 37, 40 and 52.

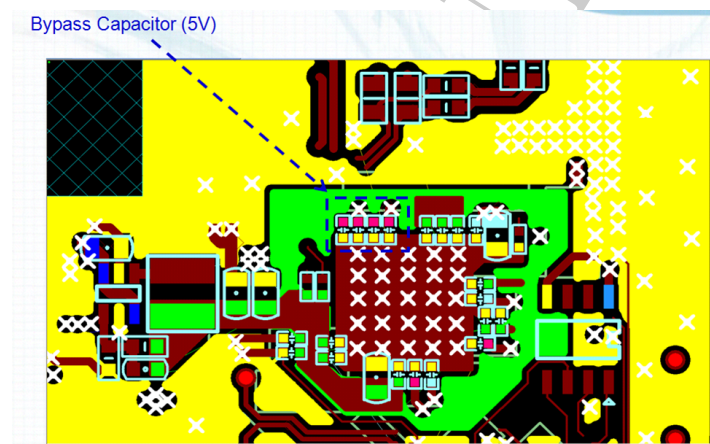


Figure 4.14: Layout for Bypass Capacitor.

Chapter 5

Others

5.1 Power over Ethernet (PoE)

5.1.1 Function Diagram

Power over Ethernet is a standard that allows you to power certain network or IP based devices over that same data cable that connects it to your network. Figure 5.1 shows the block diagram of xDSL system. The injector is placed with CPE side and transmits power through Ethernet to the CO side.

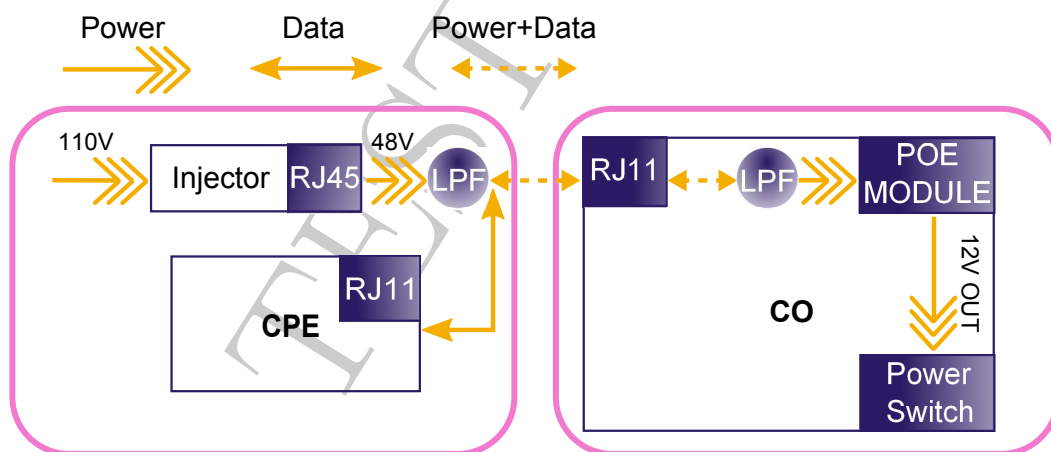


Figure 5.1: Function diagram.

5.1.2 Injector

The injector is a power supply which can export different output voltage with 100-240V input. It can be used to connect a wireless access point, IP phone, network camera or any IEEE 802.3af powered device (PD) to a switch. But the received voltage will reduce by increasing the distance from the injector to the power module. So we have to choose the appropriate output voltage to make sure the power device working. Figure 5.2 is injects with different output voltage.



Figure 5.2: Picture of a typical PoE injector.

5.1.3 Low-pass filter

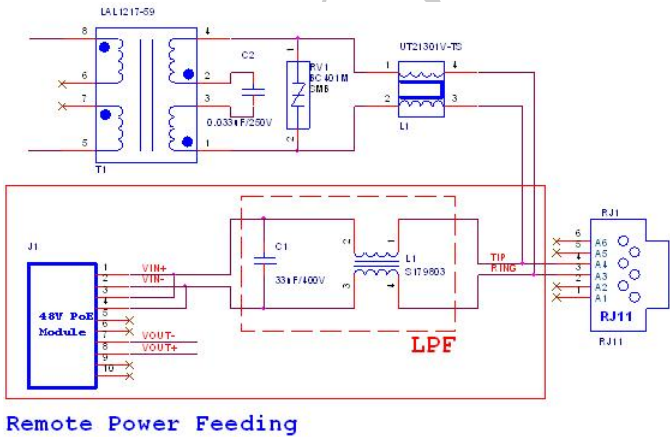


Figure 5.3: Low pass filter.

We use low-pass filters to filter the high frequency signals and keep the DC current passing on both the CO and the CPE side, or the data signals will be interfered. The low-pass filter is composed by an electric capacity and a transformer. Figure 5.3 shows the circuit of the low-pass filter on co side, and the recommended LPF components are shown as below in Table ??.

Reference	Value	Description	Part Number	Manufacturer
C1	33nF/400V	Film CAP DIP 0.033 μ F_400V	MPP 333J/400V/P	All-Rise Technic
L1	20mH	Transformer	S179803(UU9.8)	SUPREME

Table 5.1: Recommend compent

5.1.4 Power module

Behind the LPF, the DC/DC convertor power module is designed to extract power from a conventional twisted pair Category 5 Ethernet cable, conforming to the IEEE 802.3af Power-over-Ethernet standard. Then it will be used for the input voltage of the CO side device.

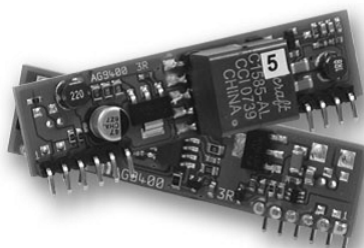


Figure 5.4: Power module.

5.2 Splitter

5.2.1 Description

In typical DSL deployments, voice and DSL services are provided by the same line of twisted-pair copper wires. Therefore it will isolate POTS signals and DSL signals. Using a splitter which is a low-pass filter will ensure optimal video, data, and voice quality by blocking interference between regular phone voice signals and broadband signals, so the isolation between POTS signals and DSL signals is most commonly achieved by installing a single CPE splitter.

5.2.2 Configuration

The following figure is a typical configuration on the CPE side.

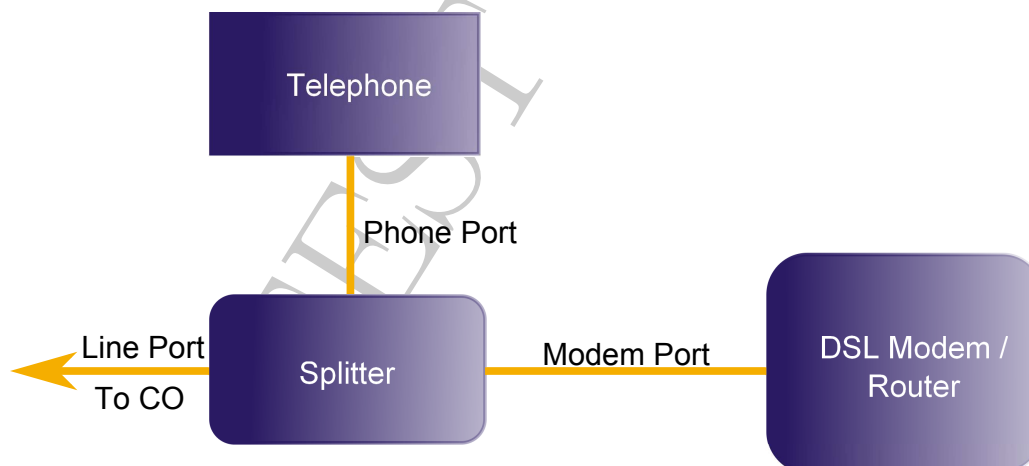


Figure 5.5: The configure of CPE side.